Luca Gammaitoni of the Noise in Physical Systems (NiPS) Laboratory at Perugia University discusses NiPS' groundbreaking experiment on the minimum energy required to operate logic gates.

Breaking the energy efficiency limit for conventional logic gates

(Left to right) Miquel Lopez Suarez, Igor Neri and Luca Gammaitoni, NiPS Laboratory

In 1961, Ralph Landauer, then working at IBM, published a paper where for the first time 'information', usually considered a purely mathematical quantity, assumed a role in physics. Specifically, Landauer's paper aimed at identifying the minimum energy required to do computation using standard thermodynamics.

Landauer initially focused on a specific operation, today known as the 'Landauer reset', that consisted of putting a binary switch – which can be in each of the two possible logic states 0 or 1 – into a given logic state. Such an operation is sometimes interpreted as 'information erasure' because it reduces the amount of information that can be associated with the binary switch: before there are two possible states, whereas after the operation there is only one possible state. According to thermodynamic law, such a reduction in the number of available states for a physical device requires a minimum energy expenditure, easily computable using previous work done by Boltzmann.

In the same paper, Landauer generalized the result associated with the reset operation to cases where there was a decrease of information between the input and the output of a computing system. This is the case of so-called logically irreversible devices. Landauer wrote: 'We shall call a device logically irreversible if the output of a device does not uniquely define the results. We believe that devices exhibiting logical irreversibility are essential to computing. Logical irreversibility, we believe, in turn implies physical irreversibility, and the latter is accompanied by dissipative effects.' [IBM Journal of Research & Development, Vol. 5, No. 3, 1961]

In fact, most standard logic operations performed on ordinary computers show 'logical irreversibility'. This is the case, for example, of the conventional 'OR' gate, where we have two bits at the input and one bit at the output. In this situation, simply knowing the value of the output is not enough to infer the actual value of the inputs.

Soon after the publication of Landauer's paper, other scientists worked to deepen and extend Landauer's principle to more general aspects of information processing. The most important result from this work is attributed to Charles Henry Bennett, also at IBM. In 1973 he published a paper titled 'Logical reversibility of computation' in which he proposed to introduce a model of computing, i.e. new devices, where there was no information decrease between the input and output of any logic operation. The motivation that led Bennett to introduce logically reversible operations was to overcome the minimum energy expenditure introduced earlier by Landauer.

Most notably, this limit was generally attributed to all logical irreversible devices, including traditional logic gates like 'OR', 'AND' and 'NAND'. Landauer and Bennett's works did not go unnoticed and a significant amount of scientific literature was produced to oppose or support the existence of such a minimum limit. It is no exaggeration to say that for more than 40 years this topic has been considered highly controversial.

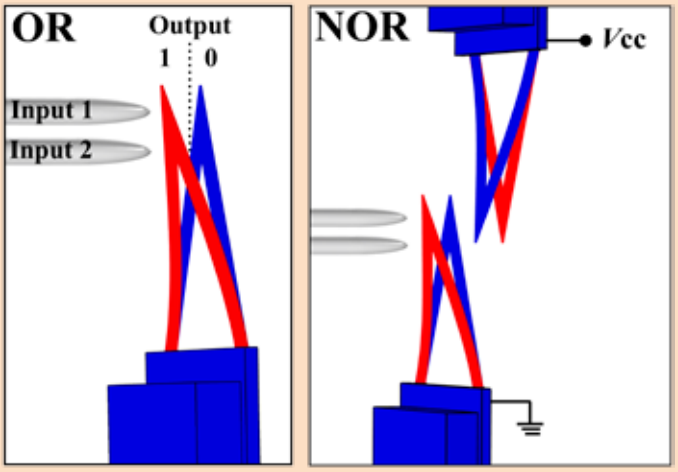
An experiment has now put an end to this controversy. It clearly shows that there is no such minimum energy limit and that a logically irreversible gate can be operated with arbitrarily small energy expenditure. Simply put, it is not true that 'logical irreversibility … implies physical irreversibility' as Landauer wrote.

The experiment, carried out by scientists in the NiPS Laboratory at the University of Perugia and recently published in Nature Communications, aimed at measuring the amount of energy dissipated during the operation of an 'OR' gate. It shows that the logic operation can be performed with an energy toll as small as 5% of the expected limit. The paper concludes that there is no fundamental limit and reversible logic is not required to operate computers with zero energy expenditure.

What are the implications of this discovery? The 'OR' logic gate used by the scientists at NiPS Laboratory is created using a micro-electromechanical cantilever, acted on by electrostatic forces. Although this cannot be considered a promising new technology for substituting the energetically expensive transistors that make our computers today, the importance of the experiment is in the demonstration that there is no limit to how much we can lower energy consumption during computation. This will change our understanding of the energy dissipation process and push research forward.

We expect this result to impact future developments in at least the following aspects:

- It will promote research towards 'zero-power' computing: the hunt for new information processing devices which consume less and less energy. This is of strategic importance for the future of the whole information and communication technology sector, which was to deal with the problem of excessive heat production during computation.
- It will call for a profound revision of the 'reversible computing' field. In fact, the experiment means that one of the main reasons for this field's existence – the presence of a lower energy limit – now no longer applies.



Logic gate operation mode. (Left) OR gate: inputs are the forces acting on the cantilever through the electrodes. The position of the cantilever tip encodes the output of the logic gate. (Right) By coupling the two cantilevers it is possible to implement the universal NOR logic gate.

ICT-Energy: reducing energy consumption across the ICT sector

The LANDAUER project forms part of ICT-Energy, a Coordination and Support Action bringing together two EU-funded research communities focusing on energy consumption in information and communication technologies: 'Towards Zeropower ICT' and 'Minimising energy consumption of computing to the limit'.

The ICT-Energy consortium comprises 10 partners, who between them coordinated 10 energy-related projects:

LANDAUER, coordinated by the **University of Perugia** (01/09/2012-31/08/2015)
Aim: to test the fundamental limits in energy dissipation during the operation of physical switches representing the basic elements of logic gates.

NANOPOWER, coordinated by the **University of Perugia** (01/08/2010 -31/07/2013)
Aim: to identify new directions for energy-harvesting technologies at the nanometre and molecular scale.

ENTRA, coordinated by **Roskilde University** (01/10/12-30/09/2015)
Aim: to promote 'energy-aware' software development using advanced program analysis and modelling of energy consumption in computer systems.

Exa2Green, coordinated by **Heidelberg University** (01/11/2012-31/10/2015)
Aim: to develop new energy-aware computing paradigms for future exascale computing.

ParaDIME, coordinated by **Barcelona Supercomputing Center** (01/10/2012-30/09/2015)
Aim: to create a processor architecture for a heterogeneous distributed system that delivers significant energy savings in data centres, for example.

PHIDIAS, coordinated by **École polytechnique fédérale de Lausanne** (01/10/2012-30/09/2015)
Aim: to achieve minimal energy consumption in wireless body sensor networks by developing power-efficient biomedical sensor nodes.

SENSATION, coordinated by **Aalborg University** (01/10/2012-29/02/2016)
Aim: to promote self-supporting systems by balancing devices' energy harvesting with the energy consumption, through energy-centric modelling and optimization tools.

TOLOP, coordinated by **Hitachi Europe** (01/09/2012-29/02/2016)
Aim: to research disruptive approaches to push significantly beyond existing power limits, by creating devices, evaluating their low-power capabilities and designing architecture to enable overall low-power circuit operation.

Green Silicon, coordinated by the **University of Glasgow** (01/08/2010-31/07/2013)
Aim: to demonstrate integrated on-chip thermoelectric energy harvesting using micro-/nano-fabricated nanostructures with improved efficiencies through the use of band-structure and phonon engineering.
SiNAPS, coordinated by **University College Cork** (01/08/2010-31/10/2013)
Aim: to develop standalone 'dust-sized' chemical sensing platforms that harvest energy from ambient electromagnetic radiation (light) and enable miniaturisation below the mm^3 barrier.

The **University of Bristol**, the other consortium partner, runs regular Energy Aware Computing (EACO) workshops, which bring together researchers and engineers interested in energy-aware computing to identify intellectual challenges which can be developed into collaborative research projects.

Technology opinion: Towards a style manual for hardware designers

Timothy Roscoe, ETH Zürich

Computer hardware is a mess. It is faster, more power-efficient, and more capable than most could have conceived when Unix was written in 1970s. But the baroque complexity of the hardware/software interface is now a major, if largely unrecognized, obstacle to progress.

The software programming manual for a modern phone system-on-chip (SoC) runs to several thousand pages of register, interrupt, descriptor, and power documentation which is often ad-hoc, incomplete, and imprecise. Really well documented SoCs (they do exist), however, present a bewildering array of intersecting address spaces, heterogeneous cores, and complex interrupt routing and power control (which may or may not be configurable, or discoverable). Millions of lines of code in the Linux kernel, for example, are there to deal with this tangle of functionality.

However, once the operating system (OS) can correctly initialize, access, and program these devices, the problems are only starting. Getting optimal performance or energy efficiency out of modern hardware appears to be beyond the state of the art of systems software. For example, a paper this year shows the wasted CPU cycles in Linux due to the scheduler's failure to adapt to different memory hierarchies.

The consequences of this are a huge programming effort spread across chip and device vendors, OS programmers, and application